REMARKS

This is in response to the Office Action of 17 April 2006. Claims 1-20 are pending in the application, Claims 1-11 have been withdrawn from consideration, and Claims 12-20 have been rejected.

By this Response and Amendment, non-elected Claims 1-11 are cancelled from this application, arguments traversing the rejections are presented, and new Claims 21-24 are added.

No new matter has been added.

In view of the amendments above and remarks below, Applicant respectfully requests reconsideration and further examination.

About The Invention

The present invention relates generally to methods and apparatus for providing access to electrical terminals of integrated circuits while those integrated circuits are still in wafer form. Various embodiments of the present invention provide a full wafer contacter that is attached to a wafer (either removably or permanently), and which provides pitch translation from the bond pads of the integrated circuits on the wafer to a larger pitch for easier access by test equipment.

Withdrawal of Election of Species Requirement of 13 December 2005

The Examiner has advised Applicant that the previous Election of Species Requirement has been withdrawn.

Rejections under 35 USC §102(b)

Claims 12-18 have been rejected under 35 USC §102(b) as being anticipated by Leas, et al., (US Patent 5,600,257). Claims 12 and 19 have been rejected under 35 USC §102(b) as being anticipated by Kwon, et al., (US Patent 5,070,297).

For at least the reasons set forth below, Applicant respectfully traverses the rejections of Claims 12-18 as being anticipated by Leas, et al., and requests that these rejections be withdrawn.

Leas, et al., disclose an apparatus and method for simultaneously testing or burning in all the integrated circuit chips on a product wafer. The apparatus comprises a glass ceramic carrier having test chips and means for connection to pads of a large number of chips on a product wafer. Voltage regulators on the test chips provide an interface between a power supply and power pads on the product chips, at least one voltage regulator for each product chip. The voltage regulators provide a specified Vdd voltage to the product chips, whereby the Vdd voltage is substantially independent of current drawn by the product chips. The voltage regulators or other electronic means limit current to any product chip if it has a short. The voltage regulator circuit may be gated and variable and it may have sensor lines extending to the product chip. The test chips can also provide test functions such as test patterns and registers for storing test results.

More particularly, Leas, et al., disclose a structure which is disposed so as to contact the pads of the integrated circuits on the wafer, and refer to this structure as a "test head" (e.g., **16** in Fig. 1; **31** in Fig. 2; **116** in Fig. 7a; and **316** in Fig. 8). Applicant respectfully notes that the test head of Leas, et al., is never actually attached (removably or permanently) to wafer **18**. In some of the embodiments of Leas, et al., the test head and wafer are urged into contact by a mechanical housing which supports the test head and the wafer. In these arrangements, the probes of the test head contact the pads of the integrated circuits, but the test head itself is not attached to the wafer. In an alternative embodiment described by Leas, et al., the test head and the wafer are again brought into contact by a mechanical clamping arrangement, but again the test head is not attached to the wafer. In other words, without the mechanical housings or clamps of Leas, et al., the test head and wafer have no means of staying together and aligned for electrical communication. The test head and wafer of Leas, et al., are not attached to each other, but rather are merely held adjacent by various mechanical apparatus.

Applicant's independent Claim 12 expressly recites "removably attaching the full wafer contacter to the wafer", which produces a structure that is not disclosed by Leas, et al. Leas, et al., do not disclose attaching a full wafer contacter to a wafer as set forth in Applicant's Claims. Leas, et al., only disclose the use of mechanical apparatus to hold the test head and wafer so that the test head and wafer are disposed adjacent each other. Leas, et al., cannot be an anticipating reference since Applicant's claimed method is not disclosed therein.

In view of the foregoing, Applicant respectfully submits that the rejection of Claims 12-18 under 35 USC §102(b) as being anticipated by Leas, et al., are improper, and requests that these rejections be withdrawn.

Applicants further submit that Leas, et al., which discloses mechanical apparatus for holding a test head adjacent to a wafer, does not suggest or provide motivation for attaching a full wafer contacter to the wafer itself.

With respect to the rejections of Claims 12 and 19 as being anticipated by Kwon, et al., for at least the reasons set forth below, Applicant respectfully traverses these rejections and requests that these rejections be withdrawn.

Kwon et al., disclose a full wafer integrated circuit testing device that tests integrated circuits formed as a wafer in conjunction with a test control unit. Probe units associate with respective integrated circuits. Probe tips on probe units communicate with respective pads on the integrated circuits. Interface circuitry selectively communicates test data between the test control unit and the integrated circuit. Test pins have positions on probe units associated with respective integrated circuit connection points for testing associated integrated circuit components. Interface circuitry includes comparators that compare signals between the integrated circuit and the test control unit . Memory components store data associated with signals from test control unit and said integrated circuit. Compliant material assures that probe tips throughout probe card positively and conductively engage integrated circuit pads of all associated integrated circuits of a wafer.

Applicant's independent Claim 12 expressly recites "removably attaching the full wafer contacter to the wafer", which produces a structure that is not disclosed by Kwon, et al. Kwon, et al., do not disclose attaching a full wafer contacter to a wafer as set forth in Applicant's Claims. Kwon, et al., disclose making contact between an integrated circuit of a wafer and the probe structures of their probe units, but never teach, suggest, or motivate attaching a full wafer contacter to the wafer. Kwon, et al., cannot be an anticipating reference since Applicant's claimed method is not disclosed therein.

In view of the foregoing, Applicant respectfully submits that the rejection of Claims 12 and 19 under 35 USC §102(b) as being anticipated by Kwon, et al., are improper, and requests that these rejections be withdrawn.

Applicants further submit that Kwon, et al., does not suggest or provide motivation for attaching a full wafer contacter to the wafer itself.

Rejections under 35 USC §103(a)

Claim 20 has been rejected under 35 USC §103(a) as being unpatentable over Kwon, et al., (US Patent 5,070,297) in view of Rostoker, et al. (US Patent 5,838,163).

Applicant respectfully traverses the rejection of Claim 20 under 35 USC §103(a) and requests that this rejection be withdrawn.

In the arguments presented above, Applicant has shown that Kwon, et al., do not disclose, suggest, or provide motivation for the invention defined by Applicant's Claims. More particularly, Kwon, et al., do not disclose removably attaching a full wafer contacter to a wafer. Rostoker, et al., is cited for its disclosure of having chips of different sizes on the same wafer. These references, taken either singularly or in combination, do not produce the invention defined by Applicant's Claims.

In view of the foregoing, Applicant respectfully submits that the rejection of Claim 20 is improper and should be withdrawn.

New Claims 21-24

New Claims 21-24, which all depend from independent Claim 12, are directed variously to the area and thickness of the full wafer contacter in relation to the area and thickness of the wafer; to the seating of a sealing ring in a groove of the full wafer contacter; and to introducing an inert gas between the full wafer contacter and the wafer. Support for these Claims can be found generally throughout the application, and more particularly at page 7, lines 20-24; page 8, lines 9-10; and page 7, lines 14-15.

Conclusion

All of the rejections in the outstanding Office Action of 17 April 2006 have been responded to, and Applicant respectfully submits that the pending Claims 12- 24 are now in condition for allowance.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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